EXHIBIT 4

Filed: April 25, 2022

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.; MICRON SEMICONDUCTOR PRODUCTS, INC.; and MICRON TECHNOLOGY TEXAS LLC,
Petitioner,

v.
NETLIST, INC.,
Patent Owner.

Case IPR2022-00236
Patent 9,824,035 B2

PATENT OWNER'S PRELIMINARY RESPONSE UNDER 35 U.S.C. § 313 AND 37 C.F.R. § 42.107

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I. INTRODUCTION

Netlist, Inc. ("Patent Owner") submits this Preliminary Response to the Petition ("Petition" or "Pet.") of Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC ("Petitioners") seeking *inter partes* review ("IPR") of U.S. Patent No. 9,824,035 ("the '035 Patent").

The Board should deny institution because Petitioners failed to meet their burden of establishing that the '035 Patent's claims are rendered obvious by the proposed combinations. Specifically, in all three Grounds, Petitioners' reliance on the Tokuhiro reference to satisfy the "*obtain timing information*" limitation is facially deficient, as Tokuhiro merely incorporates a prior art method of write leveling that the '035 Patent acknowledges is insufficient to ensure proper timing of the control and data signals received and transmitted by memory modules.

The Board should also deny the Petition pursuant to *Apple Inc. v. Fintiv, Inc.*, Case IPR2020-00019, Paper 11 (P.T.A.B., Mar. 20, 2020) ("*Fintiv I*") (precedential). By the time the Board enters a final written decision in this proceeding, significant resources will have been spent by both parties to prepare for trial in the parallel district court action. To prevent duplicative proceedings and to promote efficiency, the Board should exercise its discretion and deny institution under 35 U.S.C. § 314(a), 37 C.F.R. § 42.108(a), and 35 U.S.C. § 316(b).

II. TECHNOLOGICAL BACKGROUND

A. The '035 Patent

The '035 Patent was filed on February 7, 2017 and is a continuation of U.S. Patent No. 9,563,587, which claims priority to U.S. Provisional Patent Application No. 61/676,883, filed on July 27, 2012. The '035 Patent is related generally to memory modules, and more particularly to multi-rank memory modules and methods of operation.

For example, the '035 Patent discloses an embodiment of the invention including a module control device 116, a plurality of buffer circuits 118, and memory devices 12 that are mounted on the memory module 110. Ex. 1001, 4:18-43. The module control device 116 receives command and address signals from the system memory controller 101. *Id.*, 4:63-5:8. The module control device 116 outputs module command signals and module control signals to the memory devices and the buffer circuits, respectively. *Id.*, 5:55-67.

Figure 2A shows the logical interconnection of these components of an embodiment, while Figure 2C shows the physical arrangement of the same components on the module.

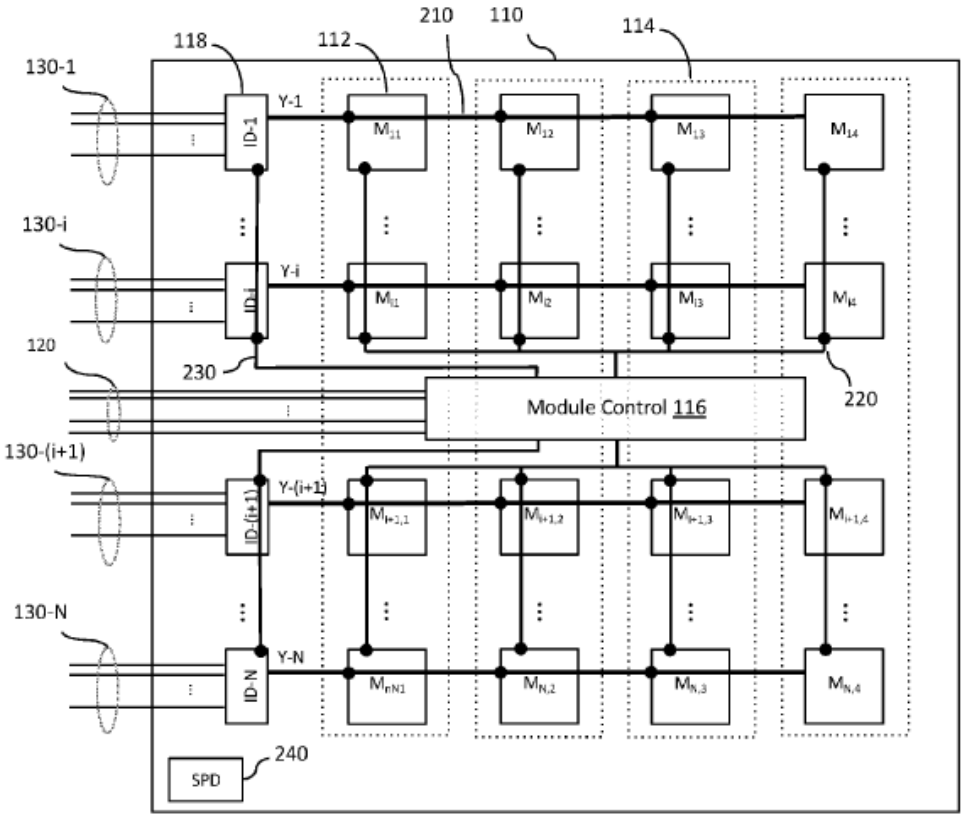


FIG. 2A

Id., Fig. 2A.

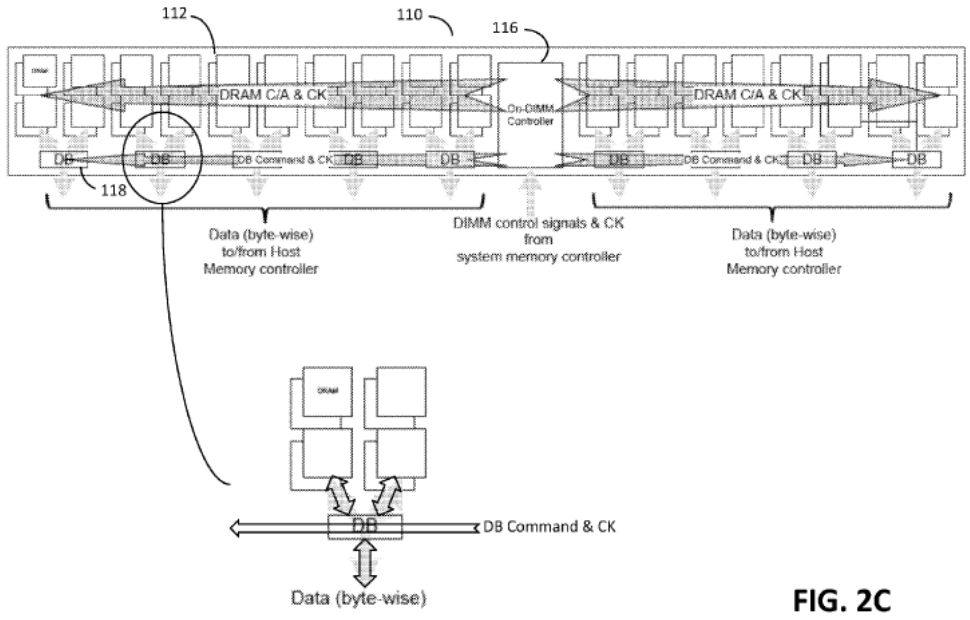


FIG. 2C

Id., Fig. 2C.

The ’035 Patent describes the need to overcome limitations of prior art memory modules and the complications posed by increasing the number of memory devices—and thus the memory density—on the memory module. For example, the specification describes the limitations of conventional read and write leveling mechanisms that were known in the prior art and used to compensate for unbalanced wire lengths:

> In some conventional memory systems, the memory controllers include leveling mechanisms for write and/or read operations to compensate for unbalanced wire lengths and memory device loading on the memory module. As memory operating speed and memory density continue to increase, however, such leveling mechanisms are also insufficient to insure proper timing of the control and/or data signals received and/or transmitted by the memory modules.

Id., 2:25-32.

Thus, the embodiments of the ’035 Patent present mechanisms for buffering command, address, timing, and data information via a module control device, a plurality of buffer circuits, and memory devices located on the memory module, resulting in modules with higher capacity and higher performance. Specifically, the ’035 Patent discloses logic circuitry in the buffer circuits that is configured to obtain timing information based on signals received during one memory operation and, in accordance with such timing information, control the timing of data and strobe signals on the data path in a subsequent memory operation. *Id.*, cl. 1.

B. The Osanai Reference (Ex. 1005)

Osanai is directed to a "Load Reduced memory module in which a considerably high data transfer rate can be realized" by including a plurality of data register buffers, data connectors, and memory chips in a line along a memory module substrate. Ex. 1005, [0008], [0018]. In this way, "a line length from a data connector to a memory chip is considerably shortened," which "makes it possible to enhance the signal quality on the module substrate." *Id.*, [0018].

The components on the disclosed memory module 100, shown in Figure 1, include the command/address/control register buffer 400, the data register buffers 300, and the memory chips 200. *Id.*, Fig. 1. The singular command/address/control register 400, shown in more detail in Figure 6, receives commands sent by the memory controller 12 over signal paths 23 (also called line L3). *Id.*, [0074-75], [0109], [0113], Figs. 1, 3, 6, 7. From these commands, the register device 400 generates control signals directed to the buffer circuits 300 and the memory devices 200. *Id.*, Figs. 1, 6. These exit the register device through ports 403 and 402, respectively, and traverse the module to reach the memory devices 200 and their corresponding data register buffers 300. *Id.*, [0120], [0113], Figs. 1, 7.

Osanai's data register buffers 300 receive write data flowing from the off-module memory controller to the memory chips 200 and read data flowing from the memory chips to the off-module memory controller. *Id.*, [0090-99], Fig. 5. In both

directions, the data is forwarded to the opposite interface and transmitted towards its destination. *Id.* In Osanai's modules, the data signals (labelled DQ) are paralleled by a strobe signal (called DQS). *Id.*, [90].

Osanai describes read and write leveling operations to adjust write timing or read timing "in consideration of a propagation time of a signal." *Id.*, [0146]. As disclosed in Osanai, write leveling operations are performed by the write leveling circuit 322 to match the phase of the strobe signal DQS to the clock signal CK. *Id.*, [0148-49]. The clock signal CK is supplied from the command/address/control register buffer 400 to both of Osanai's data register buffer 300 and the memory chip 200. *Id.*

Specifically, Osanai sends a strobe signal DQS to memory chip 200, and in response to a logical "High level" of the clock signal CK at a rising edge of the strobe signal DQS, the memory chip 200 outputs a "High level" signal back to the data register buffer 300 using a DQ input of the data register buffer 300, by which the data register 300 can find a direction of phase shift between the clock signal CK and the data strobe signal DQS. *Id.* Upon completion of write leveling, the phases of the clock signal CK and the strobe signal DQS input to the memory chip 200 are "substantially matched with each other." *Id.*, [0150-52], Figs. 14A and 14B.

Consequently, Osanai's "timing adjustment" obtained from the disclosed write leveling operation ensures that the strobe signal DQS arrives at the memory

chip 200 substantially at the same time as when the clock signal CK arrives at the memory chip 200. *See id.*

Osanai's read leveling operation determines when, for example, the input buffers INB are activated to receive data signals and strobe signals coming from the SDRAMs over L1 and L2 via terminals 341, 342, 351, and 352. *Id.*, [0146], [0153-57], Fig. 15.

> The read data DQ output from the memory chip **200** reaches the data register buffer **300**, by which the data register buffer **300** can find a time A from an input timing of the read command Read that is input as a part of the control signal DRC until the read data DQ is input. The time is … used in an adjustment of an activation timing of the input buffer circuit INB and the like.

Id., [0157].

Specifically, the data register control circuit 320 controls operations of an input buffer INB and an output buffer OUTB by generating a buffer control signal BC, and at the same time, controls operations of selectors 331 to 334 by generating a select signal SEL. *Id.*, [0094]. Osanai's "timing adjustment" of when to turn on the input buffer INB does not delay any signal going through the input buffer INB.

Osanai does not disclose that any "timing adjustment" made by write leveling circuit 322 or read leveling circuit 323 is made during any memory operation. Petitioners concede this. Pet., 36.

C. The Tokuhiro Reference (Ex. 1006)

Tokuhiro discloses a system that detects time delays during known write leveling procedures and applies such delay to adjust strobe signals sent from the system memory controller to a memory module during a write operation. Ex. 1006, 3:16-26. In this way, Tokuhiro describes that the strobe signals will arrive at substantially the same time as the clock signal sent from the system memory controller at respective SDRAMs of the memory module. *Id.,* 2:39-45, 12:59-63. Tokuhiro proposed an improved system whereby such time delays detected for the strobe signals during write leveling could be used to compute similar adjustments for the strobe signals received from respective SDRAMs of the memory module during a read operation. *Id.,* 2:54-59, 13:66-14:6, equations (1), (2-1)-(2-3), (3-1)-(3-6). Tokuhiro discloses a fly-by topology for wiring between the memory controller 12 and the SDRAM devices mounted on DIMM module 11. *Id.* at 5:24-30.

Importantly, Tokuhiro describes and incorporates known write leveling mechanisms, as disclosed in the Joint Electron Device Engineering Counsel ("JEDEC") DDR3 SDRAM Standard, JESD79-3. *Id.*, 1:22-32; 2:10-12; 2:46-49; 2:54-59. The specification describes this as follows:

> The term "write leveling function" refers to the function of sampling the clock signal CK by using the data strobe signal DQS output from the memory controller 90, detecting the phase relationship between the

> data strobe signal DQS and the clock signal CK, and adjusting (compensating) a delay time of the data strobe signal DQS.

Ex. 1006, 2:13-18.

In this way, "the difference in the delay time caused in the write operations between the memory controller . . . and the plurality of SDRAMS . . . is adjusted by employing the write leveling function." *Id*., 2:46-49. Tokuhiro notes that, although the JEDEC DDR3 standards specified such write leveling procedures for write operations, "compensations of the signal arrival time in read operations are not provided with the JEDEC standards." *Id.*, 2:54-59.

Accordingly, Tokuhiro focuses on computing time delays for compensating signals during read operations using detected delays by the known JEDEC write leveling function. Tokuhiro's first delay time control unit 23 and second delay time control unit 24 are located on the CPU 13, while the variable delay circuits are part of the control circuit units on the memory controller 12. *See id.* at Fig. 4.

Tokuhiro acknowledges that the write leveling function and variable delay circuits—which can change respective delay times of the data strobe signals—are present in the prior art and that their use in a system memory controller is also not novel. *Id.*, 1:34-2:49, Fig. 2.

D. The Takefman Reference (Ex. 1007)

Takefman discloses a system including a computer processing unit ("CPU"), a memory module, and memory bus connecting the CPU and the memory module,

as well as a co-processing unit (or input/output device). Ex. 1007, 1:48-55. The memory bus also connects the co-processing unit to the CPU. *Id.* As Takefman teaches, the I/O buses that typically connect co-processors to the computer system can "create communications bottlenecks for I/O or co-processing applications." *Id.*, 1:32-38. As a result, Takefman interfaces the co-processors via the main memory system. *Id.* at 1:42-44.

Takefman also discloses a TeraDIMM architecture embodiment including a module controller ("Rush") 301, a number of DRAM devices 302, a number of data buffer ("Bolt") devices 30, a rank of non-volatile memory devices 304, an SSD controller 305, an SPD 306, and a PIC microcontroller 307. *Id.*, 5:53-6:13. In this embodiment, data exchanged between the data bus and the DRAMs 302 flow exclusively through the Bolt devices 30, while commands to the DRAMs 302 flow through the Rush 301 on their way to the DRAMs 302. *Id.*, 5:53-6:13, Fig. 3.

Takefman's Rush 301 includes per-lane delay compensation circuits that allow for programmable launch times and lane de-skew on receipt from the Bolt devices 30. *Id.* 6:14-26. Takefman teaches that such values "may be calibrated during manufacturing and stored in onboard memory." *Id.* Takefman does not disclose that Bolt devices 30 include any delay compensation circuit, or that they obtain timing information based on signals received by the Bolt devices 30.

III. LEVEL OF ORDINARY SKILL

While Patent Owner disputes Petitioners' definition of the level of a person of ordinary skill in the art ("POSITA"), resolution of such dispute is not necessary for the Board to make a determination regarding institution. Patent Owner reserves the right to further address Petitioners' improper POSITA definition in subsequent filings, if necessary.

IV. CLAIM CONSTRUCTION

The '035 Patent's challenged claims are to be construed "using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. § 282(b)." 37 C.F.R. § 42.100(b) (Nov. 13, 2018). The Petition does not seek construction of any terms in the '035 Patent. For purposes of this filing, Patent Owner does not propose that the Board construe any claims, but Patent Owner reserves the right to do so in subsequent filings, if necessary.

V. LEGAL STANDARDS

A. Standard for Granting an IPR

The Board may only authorize an IPR be instituted where "the information presented in the petition . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a); 37 C.F.R. § 42.108(c). The petitioner bears the burden of showing that the statutory threshold is met. Office Patent Trial Practice Guide, 77 FED. REG. 48,756 (Aug. 14, 2012). A petition must provide "[a] full statement of the

reasons for the relief requested, including a detailed explanation of the significance of the evidence including material facts, and the governing law, rules, and precedent." 37 C.F.R. § 42.22(a)(2).

B. Obviousness Standard

"A patent may not be obtained . . . if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains." 35 U.S.C. § 103(a). The obviousness analysis requires several threshold inquiries.

If a single element of the claim is absent from the prior art, the claim cannot be considered obvious. *In re Rijckaert*, 9 F.3d 1531, 1534 (Fed. Cir. 1993) (reversing obviousness rejection where prior art did not teach or suggest all claim limitations); *Garmin Int'l, Inc. v. Patent of Cuozzo Speed Techs. LLC*, Case IPR2012-00001, Paper 15, at 15 (P.T.A.B. Jan. 9, 2013) (refusing to institute IPR under § 103 where the prior art did not disclose all claim limitations).

Obviousness is resolved based on factual determinations including (1) the scope and content of the prior art, (2) any differences between the claimed subject matter and the prior art, and (3) the level of ordinary skill in the art. *Graham v. John Deere Co.*, 383 U.S. 1, 17-18 (1966).

The conclusion of obviousness based on a combination of references must be supported with an explicit analysis of a reason to combine those references. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007). Such reasons must be more than "mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006).

VI. PETITIONERS FAIL TO DEMONSTRATE A REASONABLE LIKELIHOOD OF PREVAILING ON GROUNDS 1-3

A. Petitioners fail to provide evidence that any reference discloses or suggests "*obtain[ing] timing information*" as claimed (all claims).

The Petition suffers from a facial deficiency that cuts across all asserted Grounds: Tokuhiro does not disclose "*obtain[ing] timing information based on one or more signals received by the each respective buffer circuit during a second memory operation prior to the first memory operation*." Ex. 1001, cl. 1. Indeed, Tokuhiro teaches that, during the write leveling function pointed to by Petitioners as purportedly satisfying this claim element, **no memory operations can be performed at all**. For this reason, institution should be denied.

1. Petitioners concede that neither Osanai, nor Takefman discloses or suggests "*obtain[ing] timing information*."

Claim 1 of the '035 Patent (and all dependent claims) requires buffer circuits to include "*logic. . . . configured to obtain timing information based on one or more signals received by the each respective buffer circuit during a second memory*

operation prior to the first memory operation and to control timing of the respective data and strobe signals on the data paths in accordance with the timing information." Ex. 1001, cl. 1.

Petitioners concede that Osanai does not teach, disclose, or suggest logic configured to "*obtain timing information based on one or more signals received by the each respective buffer circuit during a second memory operation prior to the first memory operation*." Pet., 36 ("But Osanai does not explicitly disclose that the timing information is obtained 'during a second memory operation prior to the first memory operation.'").

Petitioners also concede that Takefman does not teach, disclose, or suggest logic configured to "*obtain timing information based on one or more signals received by the each respective buffer circuit during a second memory operation prior to the first memory operation*." Pet., 63 ("Takefman...does not expressly disclose that the timing information is obtained '*during a second memory operation prior to the first memory operation*.'") (emphasis in original).

2. Tokuhiro only discloses the method of write leveling already considered in the '035 Patent specification.

For all three Grounds, Petitioners point to Tokuhiro's write leveling function as purportedly satisfying the "*obtain timing information"* element. Pet., 36-38, 63-66, 70-71. Specifically, Petitioners state that Tokuhiro discloses write leveling techniques, which are necessary to compensate for different propagation delays

caused by memory units with different wiring lengths. Pet., 36. Petitioners point to the following passage in Tokuhiro, which discusses a time delay calculated from a known, standardized method of write leveling:

> In other words, the second delay time Dt2 for the data signal DQ input from the SDRAM can be calculated by using the first delay time Dt1 that has been set in the write leveling. Accordingly, in the second delay time control unit 24, the second delay time Dt2-x corresponding to one SDRAM-x is set by using the above-mentioned formula (3-5) so that the sum of the first delay time Dt1-x and the second delay time Dt2-x both corresponding to the relevant SDRAM-x is equal to a preset value.

Id. at 37 (citing Ex. 1006, 16:1-28).

As an initial matter, the Petition fails to prove that Tokuhiro's calculation of delay time Dt2 using a first delay time Dt1 that is "set in the write leveling" satisfies the claims' requirement that timing information obtained be "*based on one or more signals received by the each respective buffer circuit during a second memory operation prior to the first memory operation*." *See* Pet., 37. Petitioners do not show that Tokuhiro's delay time Dt1 is obtained based on signals received by the buffer circuit "*during a second memory operation prior to the first memory operation*." Instead, Petitioners point only to a delay determined during a ***write leveling procedure*** and then summarily and incorrectly conclude that such determination means that the delay was determined "*during a second memory operation*." Pet., 37 ("Consequently, Tokuhiro teaches a delay unit that obtains a first delay time from a

write operation ('*during a second memory operation*' . . . For example, Tokuhiro discloses calculating a second delay time for the read operation based on the first delay time determined by the write level operation.") (emphasis in original). This constitutes a threshold failure of proof. And even if Petitioners had attempted to show that Tokuhiro teaches obtaining timing information "*during a second memory operation*" as claimed, they could not, as described in detail below.

In its discussion of write leveling, Tokuhiro makes clear that such mechanisms were already known to a POSITA, as detailed in the Joint Electron Device Engineering Counsel ("JEDEC") DDR3 standard, JESD79-3. *See id.,* 1:22-26 ("Recently, the DDR3 . . . memory interface has been standardized as standards of a DRAM . . . by JEDEC . . . (see, *e.g.*, JDEC STANDARD (JESD79-3; DDR3 SDRAM Standard))."); *see also id.,* 2:10-45 ("For that reason, ***according to the JEDEC standards***, it is specified to employ the write leveling function ***in the DDR3 memory interface***.") (emphasis added).

Tokuhiro does not purport to teach improvements to the JEDEC write leveling mechanisms. Instead, acknowledging that JEDEC had already specified procedures for write leveling that were known at the time, Tokuhiro sought to disclose improvements to read operations. *Id.,* 2:54-59 ("Although, the DDR3 memory interface compensates the arrival time . . . in the write operations ***according to the JEDEC standards as described above***, compensations of the signal arrival time in

read operations are not provided with the JEDEC standards.") (emphasis added). Critically, none of the passages cited to by Petitioners identify any improvements to the JEDEC DDR3 write leveling functionality. *See generally* Pet., 36-38.

The '035 Patent specification also identifies known write leveling functionality—***the same write leveling functionality described as known in Tokuhiro***—as prior art and sought to improve upon it:

> In some conventional memory systems, the memory controllers include leveling mechanisms for write and/or read operations to compensate for unbalanced wire lengths and memory device loading on the memory module. As memory operating speed and memory density continue to increase, however, such leveling mechanisms are also insufficient to insure [sic] proper timing of the control and/or data signals received and/or transmitted by the memory modules.

Ex. 1001, 2:25-32. Just as in Tokuhiro, the specification states that such write leveling mechanisms are used "to compensate for unbalanced wire lengths." *Id.*; *see also* Ex. 1006, 1:63-2:9.

Thus, Petitioners point to the known JEDEC DDR3 write leveling functionality as the only support for their claim that the "*obtain timing information*" limitation is met. Pet., 36-38. As described below, the JEDEC DDR3 write leveling functionality does not obtain timing information "*based on one or more signals received by the each respective buffer circuit during a second memory operation prior to the first memory operation*" as required in claim 1 of the '035 Patent.

3. Tokuhiro does not disclose or suggest "*obtain[ing] timing information*" as claimed.

The JEDEC DDR3 standard,[1] identified by Tokuhiro as teaching a known method of write leveling, describes a write leveling procedure that is performed by the system memory controller to align strobe (DQS) and clock (CK) signals arriving at each memory device located on a DDR3 memory module. *See* Ex. 2004, 38-41.[2] The alignment timing is used subsequently by the system memory controller to adjust data strobe (DQS) signals when performing memory write operations to the DDR3 memory module:

[1] JEDEC's JESD79-3 was published in June 2007. *See* Ex. 2003, JEDEC Standard DDR3 SDRAM Standard JESD79-3 (June 2007). JESD79-3A, the first revision of JESD79-3, was published in September 2007. *See* Ex. 2004, JEDEC Standard DDR3 SDRAM Specification JESD79-3A (September 2007). Tokuhiro was filed on September 12, 2008. Citations to JESD79-3 hereinafter will be to JESD79-3A. Citations to both versions are included herein for the Board's consideration. Petitioners rely on and cite to JEDEC's JESD79-3C, published November 2008. *See* Pet., Ex. 1013.

[2] *See* Ex. 2003, 38-41 (June 2007).

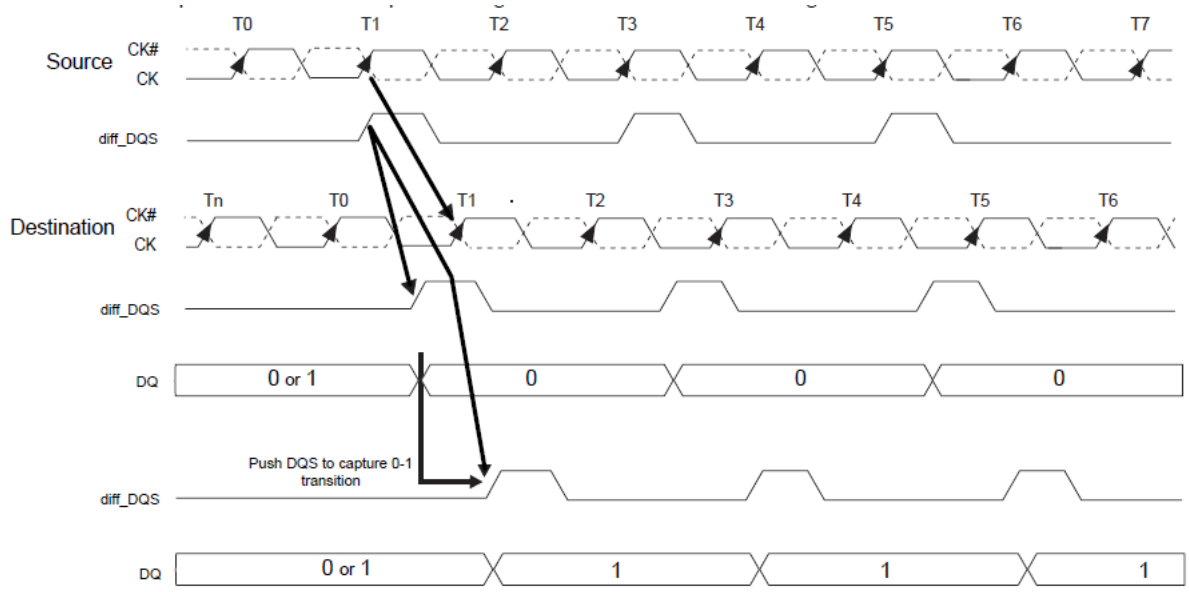


Figure 14 — Write Leveling Concept

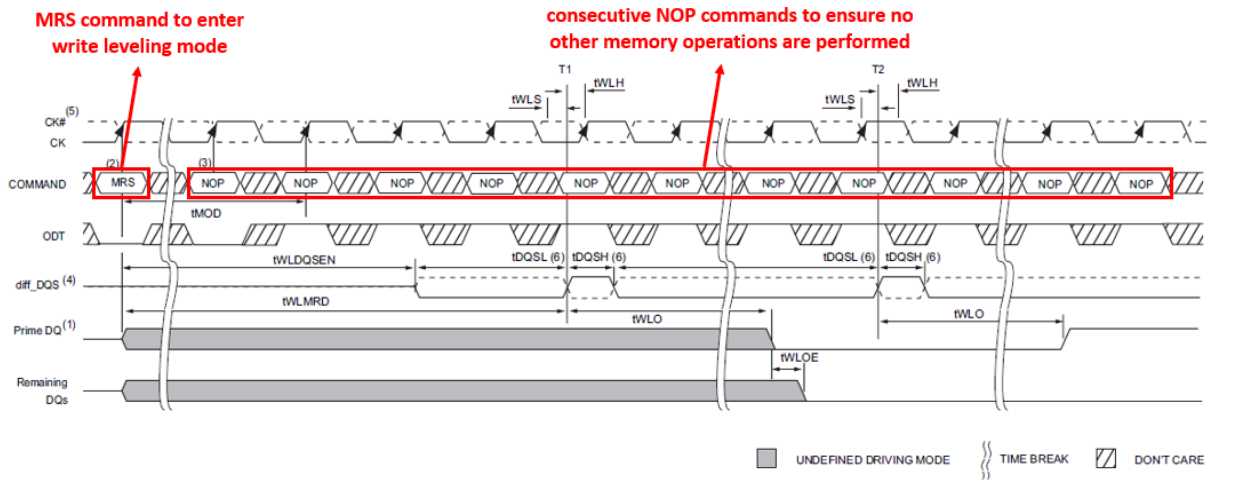
See Ex. 2004, Fig. 14 (September 2007).[3] The write leveling mode of operation is enabled or disabled using a Mode Register Set (MR1) command. *Id.* at 41.[4]

Importantly, however, during the write leveling mode, JESD79-3 teaches that the memory module is prohibited from performing any memory operations, at the direction of the memory controller, or otherwise. For example, JESD79-3A states that, "[w]ith entering write leveling mode, the DQ pins are in undefined driving mode. ***During write leveling mode, only NOP or DESELECT commands are allowed, as well as an MRS command to exit write leveling mode***." *Id.* at 39

[3] *See* Ex. 2003, Fig. 14 ("Write leveling concept").

[4] *See* Ex. 2003, 41 ("After the RTT is switched off, disable Write Level Mode via MR command").

(emphasis added).[5] Timing diagrams confirm that the system memory controller sends consecutive NOP commands to ensure that the memory controller does not issue any other memory operations until after issuing the MRS command to exit the write leveling procedure:



NOTES:
1. DRAM has the option to drive leveling feedback on a prime DQ or all DQs. If feedback is driven only on one DQ, the remaining DQs must be driven low, as shown in above Figure, and maintained at this state through out the leveling procedure.
2. MRS: Load MR1 to enter write leveling mode.
3. NOP: NOP or Deselect.
4. diff_DQS is the differential data strobe (DQS, DQS#). Timing reference points are the zero crossings. DQS is shown with solid line, DQS# is shown with dotted line.
5. CK, CK# : CK is shown with solid dark line, where as CK# is drawn with dotted line.
6. DQS, DQS# needs to fulfill minimum pulse width requirements tDQSH(min) and tDQSL(min) as defined for regular Writes; the max pulse width is system dependent.

Figure 15 — Timing details of Write leveling sequence [DQS - DQS# is capturing CK - CK# low at T1 and CK - CK# high at T2

[5] *See* Ex. 2003, 39 ("With entering write leveling mode, the DQ pins are in undefined driving mode. During write leveling mode, only NOP or DESELECT commands are allowed.").

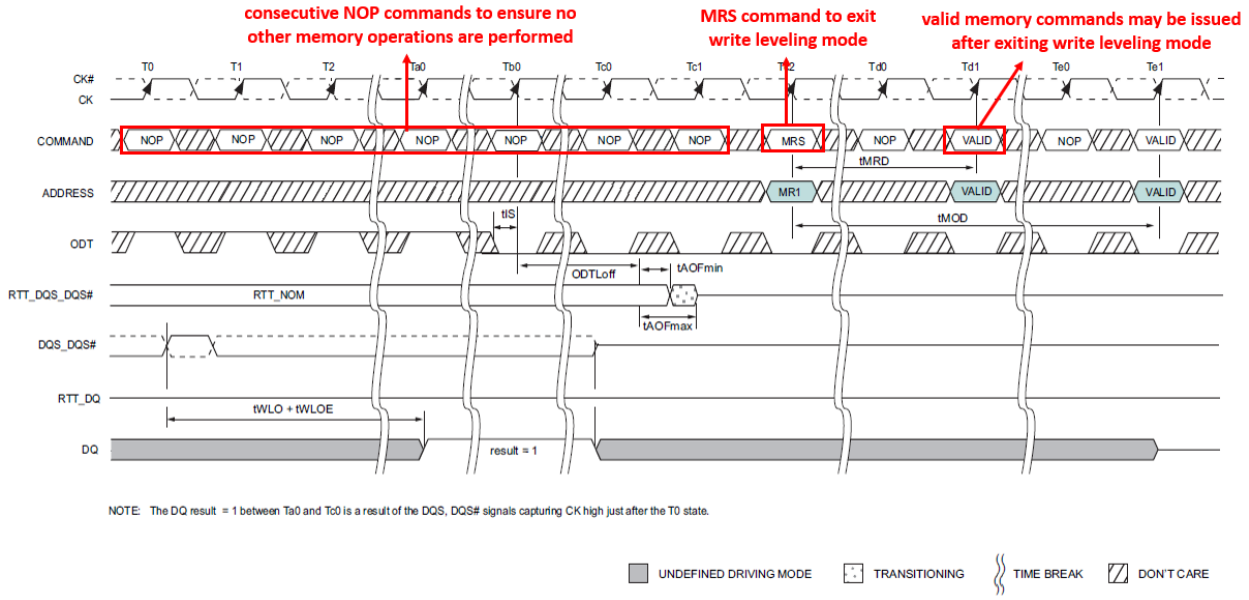


Figure 16 — Timing details of Write leveling exit

Id., Figs. 15, 16 (annotations added).[6]

Only upon exiting the write leveling mode can any subsequent memory operation (*e.g.,* a memory read or write operation) resume. *See id.,* Fig. 16.[7]

[6] *See* Ex. 2003, Figs. 15, 16.

[7] *See* Ex. 2003, Fig. 16.

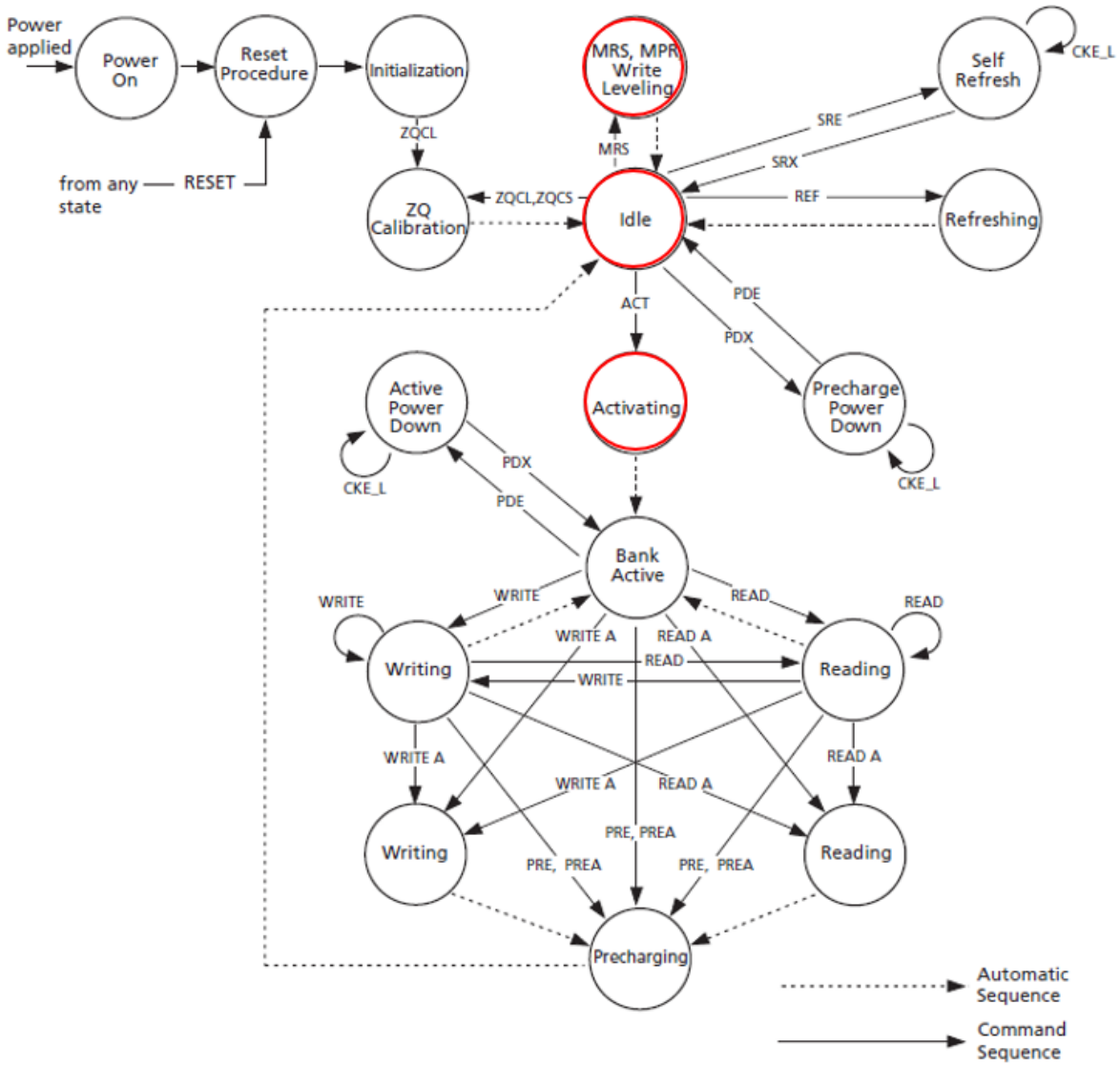


Figure 1 — Simplified State Diagram

See also id., Fig. 1 (annotated) (showing a simplified state diagram of DDR3 SDRAM wherein the write leveling procedure can only be entered from an idle state; upon exiting the write leveling mode, the memory device returns to an idle

state from which a memory read or write operation can only be performed once the memory device enters an active state using an ACT command).[8]

Petitioners point to Tokuhiro's disclosure of a delay time that "can be calculated by using the first delay time Dt1 that has been set in the write leveling" as support for the contention that the "*obtain timing information*" limitation is met. Pet., 37. However, as described above, any delay time set in write leveling is not timing information obtained "*during a . . . memory operation*" as claimed because no memory operations can be performed during the write leveling function taught in Tokuhiro and JESD79-3. Importantly, it is not until ***after*** the write leveling procedure has been performed that commands for memory operations are issued. *See* Ex. 2004, Fig. 16.[9] Thus, any timing information determined ***during*** write leveling in Tokuhiro is not obtained during any "*memory operation*" as required by the claims. As a result, Tokuhiro does not disclose or suggest a buffer circuit including

[8] *See* Ex. 2003, Fig. 1 (showing a simplified state diagram of DDR3 SDRAM wherein the write leveling procedure can only be entered from an idle state; upon exiting the write leveling mode, the memory device enters an idle state from which a memory read or write operation can only be entered once activate using an ACT command).

[9] *See* Ex. 2003, Fig. 16.

logic configured to "*obtain timing information based on one or more signals received by the each respective buffer circuit* ***during a second memory operation*** *prior to the first memory operation*." Ex. 1001, cl. 1 (emphasis added).

VII. THE FINTIV FACTORS FAVOR DISCRETIONARY DENIAL OF INSTITUTION UNDER 35 U.S.C. § 314(a)

By the time the Board enters a final written decision in this proceeding, both parties will have spent significant time and resources resolving issues relating to the validity of the '035 Patent in the parallel district court action. The Board should exercise its discretion to deny the petition under *Fintiv I*, IPR2020-00019, Paper 11.

A. *Fintiv* Factor #1: Whether the district court granted a stay or evidence exists that one may be granted if a proceeding is instituted.

Petitioners offer no evidence that the district court would grant a stay if an IPR is instituted; indeed, Petitioners concede they "do not know if the district court will stay the case." Pet., 74. Thus, this factor is neutral. *Apple Inc. v. Fintiv, Inc*., Case IPR2020-00019, Paper 15 at 12 (P.T.A.B. May 13, 2020) ("*Fintiv II*") (informative) (determining that Factor 1 is neutral when a stay motion has not been addressed by the district court).

B. *Fintiv* Factor #2: Proximity of the district court's trial date to the Board's projected statutory deadline for a final written decision.

As *Fintiv I* explains, "[i]f the court's trial date is at or around the same time as the projected statutory deadline ***or even significantly after the projected statutory deadline***, the decision whether to institute will likely implicate other factors

discussed herein . . .” *Fintiv I*, Paper 11 at 9 (emphasis added). Here, no trial date has been set in the district court action. Pet., 74. Thus, this factor is neutral, and the decision to institute should implicate the other *Fintiv* factors. At most, this factor should only have a “slight” impact on the overall determination. *See Taiwan Semiconductor Mfg. Co., Ltd. v. Fraunhofer Gesellschaft Zur Forerderung Der Angewandten Forchung Ev*, Case IPR2020-01669, 2021 WL 14332363, at *11 (P.T.A.B. Apr. 15, 2021) (“Because it is unclear whether the trial will occur before, contemporaneously with, or after the final written decision, this factor weighs slightly against exercising our discretion to deny the Petition.”).

C. *Fintiv* Factor #3: Investment in the parallel proceeding by the district court and the parties at the time of the institution decision.

Petitioners predicted, without basis, that “the [district] court is unlikely to invest any resources on the grounds raised in this petition, either before or after the scheduled institution date.” Pet., 73. Petitioners are wrong on several counts. After this Petition was filed, the district court ordered four rounds of claim construction briefing, set a tutorial for May 12, 2022, and ordered a claim construction hearing to also commence May 12, 2022. Ex. 2005. These claim construction briefings, tutorial, and hearing specifically address the ’035 Patent and several disputed terms from claims asserted in both the parallel litigation and challenged in the instant Petition. *See* Ex. 2006, Joint Claim Construction Chart (Apr. 14, 2022). It is also worth noting that the parties have already expended extensive resources preparing

voluminous infringement contentions and invalidity contentions and references. Ex. 2007.

The institution deadline for this proceeding is July 25, 2022. By that time, the parties and the district court will have expended significant additional resources, having reviewed and digested the multiple rounds of claim construction briefing, and having concluded the tutorial and claim construction hearing on May 12, 2022. Given the approximately two and one-half months between the May 12th claim construction hearing and the July 25th institution deadline, it is reasonable to presume that the district court will issue its claim construction decision prior to the institution deadline, and Petitioners have provided no evidence or argument to indicate otherwise. The completion of the claim construction process at the district court is an objective indication of the advanced stage of the parallel litigation that favors denial of institution. *See Fintiv I*, Paper 11 at 10. ("[D]istrict court claim construction orders may indicate that the court and parties have invested sufficient time in the parallel proceeding to favor denial.").

Moreover, when considering this third factor, *Fintiv* directs the Board to consider not only the investment of the parties and the court, but also whether "the petitioner filed the petition expeditiously, such as promptly after becoming aware of the claims being asserted." *See Fintiv I*, Paper 11 at 11. Here, Petitioners failed to act diligently in filing their IPR petitions. Specifically, Patent Owner filed its

complaints alleging patent infringement of four patents against Petitioners on April 28, 2021. Ex. 2008. Petitioners, however, waited eight months to file the first set of IPR petitions against the '035 and '608 Patents on December 23, 2021. *See* IPR2022-00236 and -00237. Petitioners then filed another IPR petition approximately a month later against U.S. Patent No. 8,301,833 on January 14, 2022. *See* IPR 2022-00418. Petitioners then filed two more IPR petitions on January 14, 2022—more than eleven months after the filing of Patent Owner's complaints—challenging the claims in U.S. Patent No. 10,489,314. *See* IPR2022-00744 and -00745. Overall, Petitioners lacked diligence in filing their IPR petitions against Patent Owner, which increased the investment of time and resources by the court and parties in the parallel district court proceedings. *See Fintiv I*, Paper 11 at 11. ("[N]otwithstanding that a defendant has one year to file a petition, it may impose unfair costs to a patent owner if the petitioner… waits until the district court trial has progressed significantly before filing a petition at the Office.").

Factor 3 therefore weighs in favor of exercising discretionary denial of institution.

D. *Fintiv* Factor #4: Overlap and potential conflict between issues raised in the petition and in the parallel district court proceeding.

As the Board found in *Fintiv*, "if the petition includes the same or substantially the same claims, grounds, arguments, and evidence as presented in the parallel proceeding, this fact has favored denial." *Fintiv I*, IPR2020-00019, Paper 11 at 12.

Here, Petitioners have asserted the exact same references against every asserted claim in the parallel litigation. Thus, there is substantial overlap in the claims, grounds, arguments, and evidence. *See* Ex. 2009, Defendants' Preliminary Invalidity Contentions at 21 (Nov. 5, 2021) (generally asserting obviousness combinations including Osanai, Tokuhiro, and Takefman).

Petitioners argue incomplete overlap of issues due to their Petition addressing three claims not asserted in the parallel litigation. Pet., 73. However, the Board has recognized that "if a petition involves the same prior art challenges but challenges claims in addition to those that are challenged in the district court, it may still be inefficient to proceed because the district court may resolve validity of enough overlapping claims to resolve key issues in the petition." *Fintiv I*, Paper 11 at 13. More importantly, Petitioners' argument fails because any challenge involving non-overlapping claims depends on the dissimilarity of the claims challenged in the petition to those at issue in the district court, and Petitioners did not argue the dissimilarity of the three non-overlapping claims. *Id., citing Next Caller, Inc. v. TrustID, Inc.,* Case IPR2019-00961, Paper 10 at 14 (P.T.A.B. Oct. 16, 2019) (denying institution even though two petitions jointly involve all claims of patent and district court involves only a subset of claims because the claims all are directed to the same subject matter and petitioner does not argue that the non-overlapping claims differ significantly in some way). All claims at issue in the Petition are

generally directed to a memory module. Accordingly, the district court litigation and this Petition present the same or substantially same claims, grounds, arguments, and therefore favors discretionary denial.

Petitioners separately argue that this fourth factor weighs "strongly in favor of institution" because they stipulated not to pursue invalidity on the same grounds in the litigation if the Board institutes trial in this proceeding. Pet., 72. However, the breadth of the stipulation affects the weight given in the discretionary denial analysis. For example, a petitioner stipulating not to pursue the "same grounds" presented in a petition only marginally favors not exercising discretionary denial, while a petitioner stipulating not to pursue "any ground raised or that could have been raised" weighs strongly in favor of not exercising discretionary denial. *Sand Revolution LLC v. Continental Intermodal Group-Trucking II, LLC*, Case IPR2019-01393, Paper 24, 11-12 (P.T.A.B. Jun. 16, 2020) (informative); *Sotera Wireless, Inc. v. Masimo Corp.*, Case IPR 2020-01019, Paper 12, 18-19 (P.T.A.B. Dec. 1, 2020) (precedential as to § II.A).

Here, Petitioners have not stipulated that they will not raise grounds in the litigation that "could have been raised" in the Petition. Rather, Petitioners have only disclaimed assertion of grounds involving the three particular references asserted in the Petition. Ex. 1016. Moreover, Petitioners expressly reserved the right to rely on Osanai, Tokuhiro, and Takefman with respect to "other issues" in the district court

matter, such as, among other things, for background information or to support claim construction and non-infringement arguments. *Id*. at 2. Thus, potential overlap in arguments and evidence still remain despite Petitioners' (limited) stipulation. Therefore, this factor is neutral in determining whether to deny institution. *See, e.g., Apple Inc. v. Pinn, Inc*., PGR2020-00066, 2020 WL 7233481, at *9 (P.T.A.B. Dec. 8, 2020) (viewing Factor 4 as neutral given some remaining overlap in arguments and evidence even after submission of limiting stipulation by Petitioner).

E. *Fintiv* Factor #5: Whether the petitioner and the defendant in the parallel district court proceeding are the same party.

As in *Fintiv*, this factor weighs in favor of denial because Petitioners and defendants in the parallel district court proceeding are one and the same. *Fintiv I*, Paper 11 at 11.

F. *Fintiv* Factor #6: Other circumstances that impact the Board's exercise of discretion, including the merits.

As explained in greater detail above, the Board should deny institution of this proceeding because Petitioners have not demonstrated a reasonable likelihood of success due to fatal, facial flaws in the Petition. *See Fintiv I*, Paper 11 at 15 ("if the merits of the grounds raised in the petition are a closer call, then that fact has favored denying institution when other factors favoring denial are present.").

* * *

In consideration of the totality of the above factors, the Board should exercise discretion to deny institution under the *Fintiv* decision.

VIII. CONCLUSION

For the foregoing reasons, Patent Owner respectfully requests the Board deny Petitioners' request for IPR of U.S. Patent No. 9,824,035.

Dated: April 25, 2022

Respectfully Submitted,

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CERTIFICATE OF WORD COUNT

Under the provisions of 37 C.F.R. § 42.24(d), the undersigned hereby certifies that the Microsoft Office word count for the foregoing Patent Owner's Preliminary Response Under 35 U.S.C. § 313 and 37 C.F.R. § 42.107, excluding the table of contents, table of authorities, claim listing, certificate of word count, and certificate of service, totals 6,196 words, which is less than the 14,000 words allowed under 37 C.F.R. § 42.24(b)(1).

Dated: April 25, 2022

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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e), I certify that I caused to be served on the counsel for Petitioners a true and correct copy of the foregoing Patent Owner's Preliminary Response Under 35 U.S.C. § 313 and 37 C.F.R. § 42.107, by electronic means on April 25, 2022, by delivering a copy via electronic mail to the attorneys of record for the Petitioners as follows:

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